Academic Personnel Short Profile / Short CV

University:	Cyprus University of Technology
Surname:	MICHAIL
Name:	HARRIS (HARALAMBOS)
Rank/Position:	SPECIAL TEACHING STAFF (STS)
Faculty:	Faculty of Engineering and Technology
Department:	Department of Electrical Engineering, Computer Engineering and Informatics
Scientific Domain: *	DIGITAL ELECTRONICS, HARDWARE DESIGN, CRYPTOGRAPHY

** Field of Specialization*

Academic qualifications (list by highest qualification)

Qualification	Year	Awarding Institution	Department	Thesis title (Optional Entry)
Ph.D.	2009	University of Patras	Dept. of Electrical & Computer Engineering	*"Optimization of cryptographic and data intensive applications in reconfigurable platforms for throughput and power dissipation"*
MSc. in "Integrated Software and Hardware Systems"	2011	University of Patras	Dept. of Electrical & Computer Engineering	
Diploma (Bsc/Msc)	2004	University of Patras	Dept. of Electrical & Computer Engineering	

Employment history in Academic Institutions/Research Centers – List by the three (3) most recent				
Period of employment		**Employer**	**Location**	**Position**
From	**To**			
1/2012	6/2019	Cyprus University of Technology	Limassol, Cyprus	Special Teaching Staff
9/2009	12/2011	Computer Engineering and Informatics Dpt. , University of Patras	Patras, Greece	Adjunct Assistant Professor
5/2009	12/2011	Electrical & Computer Engineering Dpt. , University of Patras,	Patras, Greece	Post-Doc Researcher
9/2009	12/2011	Mechanical Engineering Dpt, Technological Institute of Patras	Patras, Greece	Adjunct Assistant Professor
2/2010	6/2011	Department of Speech and Language Therapy Dpt, Technological Institute of Patras	Patras, Greece	Adjunct Assistant Professor
2/2010	6/2010	Museology, Museography and Exhibition Design Dpt, Technological Institute of Patras	Pyrgos, Greece	Adjunct Assistant Professor
9/2009	12/2011	Mechanical Engineering Dpt, Technological Institute of Patras	Patras, Greece	Adjunct Assistant Professor

PUBLICATIONS						
Ref #	**Year**	**Title**	**Other Authors**	**Journal/ Publisher/ Conference**	**Vol**	**Pages**
1	2016	*Area-Throughput Trade-Offs for SHA-1 and SHA-256 Hash Functions' Pipelined Designs*	*G. S. Athanasiou, V. Kelefouras, G. Theodoridis, T. Stouraitis and C.E Goutis*	*Journal of Circuits, Systems and Computers (JCSC), World Scientific Publishers Company*	*Vol 25, Iss. 4*	*pp 1-35*
2	2016	*Design and Implementation of Totally-Self Checking SHA-1 and SHA-256 Hash Functions' Architectures*	*G.S. Athanasiou, G. Theodoridis, A. Gregoriades and C. E. Goutis*	*Microprocessors and Microsystems, Elsevier*	*vol. 45, Part B*	*pp. 227–240*
3	2014	*On the Development of High-Throughput and Area-Efficient Multi-mode Cryptographic Hash Designs in FPGAs*	*G.S. Athanasiou, G. Theodoridis and C. E. Goutis*	*Integration, the VLSI Journal*	*vol.47, Is. 4*	*pp. 387–407*
4	2013	*Optimizing the SHA-512 Cryptographic Hash Function On FPGAS*	*G.S. Athanasiou, G. Theodoridis and C. E. Goutis*	*IET Computers & Digital Techniques*	*vol. 8, Iss.2*	*pp. 70–82*
5	2012	*On the exploitation of a high-throughput SHA-256 FPGA design for HMAC*	*G. S. Athanasiou, V. Kelefouras, G. Theodoridis and C. E. Goutis*	*ACM Transactions on Reconfigurable Technology and Systems (TRETS)*	*vol. 5, no.1*	*pp. 2:1–2:28*
6	2011	*A Memory Efficient Fast Fourier Transform (FFT) Methodology*	*V. Kelefouras, G. Athanasiou, N. Alachiotis, A. Kritikakou, and C.E. Goutis*	*IEEE Transactions on Signal Processing*	*vol.59, no 12*	*pp. 6217–6226*
7	2010	*Cryptography in the Dawn of IPv6*		*IEEE Goldrush Newsletter*	*vol. Dec 2010*	*pp. 17*
8	2009	*An RNS Architecture of an Fp Elliptic Curve Point Multiplier*	*D.M. Schinianakis, A.P. Fournaris, A.P. Kakarountas and T. Stouraitis*	*IEEE Transactions on Circuits and*	*vol.56, no 6*	*pp. 1202–1213*

				Systems I		
9	*2009*	*A Top-Down Design Methodology for Implementing Ultra High-Speed Hashing Cores*	*A. P. Kakarountas, A. S. Milidonis and C. E. Goutis*	*IEEE Transactions on Dependable and Secure Computing*	*vol. 6, no.4*	*pp. 255–268*
10	*2007*	*Server Side Hashing Core Exceeding 3 Gbps of Throughput*	*G.A. Panagiotakopoulos, V.N. Thanasoulis, A.P. Kakarountas, C.E. Goutis*	*International Journal of Network Security (special issue),*	*Vol. 1, Nos. 1/2/3*	*pp. 43–53*
11	*2006*	*High-Speed FPGA Implementation of Secure Hash Algorithm for IPSec and VPN Applications*	*A.P. Kakarountas, A. Milidonis, G. Theodoridis, C.E Goutis*	*Journal of Supercomputing, Springer Science*	*vol. 37*	*pp. 179–195*
12	*2010*	*Authentication with RIPEMD-160 and other alternatives: A Hardware Design Perspective*	A. Gregoriades, V. Kelefouras, G. Athanasiou, A. Kritikakou and C. Goutis	Advanced Technologies, IN-TECH Inc. Publishers	Book chapter ISBN: 978-953-307-067-4	pp. 103-124
13	*2005*	*A Low-Power and High-Throughput Implementation of the SHA-1 Hash Function*	A.P. Kakarountas, O. Koufopavlou, C.E. Goutis	ISCAS'05, Kobe, Japan	*Conference*	pp. 4086-4089
14	*2008*	*A Segmented High-Speed Counter Based on the Use of Redundant Bits*	A. Kakarountas, G. Theodoridis and C.E. Goutis	VLSI-SOC'08, Rhodes, Greece	*Conference*	pp. 42-48
15	*2012*	On the development of totally self-checking hardware Design for the SHA-1 hash function	G. S. Athanasiou, A. Gregoriades, G. Theodoridis and C. Goutis	SECRYPT'12, Rome, Italy	*Conference*	pp. 309-313
16	*2014*	Distribution of Cultural Content through Exploitation of Cryptographic Algorithms and Hardware Identification	C. Louca, D. Gavrilis, A. Gregoriades, L. Anastasiou, and M. Ioannides	Euromed 2014, Lemesos, Cyprus	*Conference*	pp. 156-165

17	*2014*	Cultural Heritage Object Metadata Enrichment in an Integrated Aggregation Environment	D. Gavrilis, M. Ioannides, C.Papatheodorou and C. Dallas	Euromed 2014, Lemesos, Cyprus	*Conference*	pp. xxx-xxx
18	*2015*	Pipelined SHA-3 Implementations on FPGA: Architecture and Performance Analysis	L. Ioannou and A. G. Voyiatzis	CS^2 Workshop/HiPEAC, Amsterdam, Netherlands	*Conference*	pp. 9-24
19	*2015*	High Performance Pipelined FPGA Implementation of the SHA-3 Hash Algorithm	L. Ioannou and A. G. Voyiatzis	MECO 2015, Budva, Montenegro	*Conference*	pp. xxx-xxx
20	*2018*	Design and Validation of an Agent-Based Driving Simulator	A. Gregoriades, M. Pampaka, Maria Viugova	SummerSim '18, Bordeaux, France	*Conference*	Article 6:1-6:12

Exhibitions (where applicable). List five (5) more recent and other five (5) selected. (max total 10)

Ref #	Period	Organization	Title of Position or Service	Key Activities	Others
1	2012,2014	EUROMED 2012 EUROMED 2014	Member of the Local Organization Committee	Member of the Local Organization Committee, Reviewer	

Research Projects. List the five (5) more recent and other five (5) selected (max total 10)

Ref #	Date	Title	Funded By	Project Role*
1	2004-2008	EASY: Energy-Aware SYstem-on-Chip design of the HIPERLAN/2 standard	European Union funding	*Researcher*

2	2004-2009	Methodologies for finding heterogeneous system's architectures in system-on-chip with reconfigurable array architectures for data intensive applications	Greek Secretariat of Research and Technology and EU funding	*Researcher*
3	2004-2009	Methodologies for finding reconfigurable architectures for embedded system design	Greek Ministry of National Education and Religious Affairs funding	*Researcher*
4	2004-2009	MARLOW: A central market place for dissemination of low power microelectronics	European Union funding	*Researcher*
5	2009-2012	Microelectronic circuits for Lab-On-Chip instruments for molecular analysis for genetic and environmental applications	Hellenic Technology Clusters Initiative (Corallia)	*Researcher*

**Project Role: i.e. Scientific/Project Coordinator, Research Team Member, Researcher, Assistant Researcher, other*

Academic Consulting Services and/or Participation in Councils / Boards/ Editorial Committees. List the five (5) more recent (Optional Entry)				
Ref. Number	**Period**	**Organization**	**Title of Position or Service**	**Key Activities**
1	2012-present	Journal of Wireless Communications, Sanford Inter Science Press	Member of the Editorial Board	Member of the Editorial Board, Reviewer
2	2012-present	More than 20 conferences	Member of the Technical Program Committee	Member of the Technical Program Committee, Reviewer
3	2005-present	More than 40 journals and conferences	Reviewer	Article reviewing

4	2012	Ministry of Education, Lifelong Learning and Religious Affairs, Greece	Evaluator for funding proposals of the call "Program for Upgrading Knowledge and Expertise of University Post-graduates"	Evaluator of Research/Educational Proposals for Funding

Awards / International Recognition (where applicable). List the five (5) more recent and other five (5) selected. (max total 10) (Optional Entry)			
Ref. Number	**Date**	**Title**	**Awarded by:**
1	2005	"Efficient small-sized implementation of the keyed-hash message authentication code"	"2005 IEEE Region 8 Student Paper Contest" awarded 3rd place
2	2004-2018	Citations in research work : 523	*Found through Google scholar on 15/05/2019*

Other Achievements. List the five (5) more recent and other five (5) selected. (max total 10) (Optional Entry)			
Ref. Number	**Date**	**Title**	**Key Activities:**
1	2005-2008	Scholarship for PhD studies through «PENED 2003», project «Methodologies for finding heterogeneous system's architectures in system-on-chip with reconfigurable array architectures for data intensive applications», PENED'03 – 03ED507, Greek Secretariat of Research and	Scholarship for PhD studies

		Technology funding (12/2005-12/2008)	
2	2012	Scholarship for Post-Doc studies by The Matsumae International Foundation, Japan “Research Fellowship Program”, Project “High Performance Hash Cores for IPv6”, in collaboration with University of Tsukuba, Japan.	The Matsumae International Foundation, Japan “Research Fellowship Program”